B1 Cont.

gas. See Evans, et al., "High Performance CMOS Devices with 20 Å Engineered Oxynitride Gate Dielectrics", Paper Presented at Semicon Korea Technical Symposium, (February 2000).--

REMARKS

Upon entry of the above amendments, Claims 1-23 will remain pending in this application. The amendments to the specification are typographical in nature.

No new matter is incorporated by this Amendment.

Rejections under 35 U.S.C. § 102

Claims 1-10, 13-14, and 18-23 are rejected under 35 U.S.C. § 102(e) as purportedly anticipated by Oya et al., U.S. Patent No. 6,479,349.

Applicants respectfully traverse.

For the record, Applicants note the distinction between nitrous oxide (N_2O) and nitric oxide (NO) as the Office Action is not clear in its use of these terms. The Claims all designate nitric oxide (NO) in the claimed methods. Applicants further note that a diffusion furnace operating at about 900-1000°C is not the same as a chemical vapor deposition furnace operating at about 800°C or less.

Oya et al. fails to anticipate the claims. Oya et al. only discloses nitric oxide (NO) in the context of a heat annealing step that occurs in a diffusion furnace in the first embodiment described at col. 6, line 66 through col. 7, line 29. In this embodiment, nitric oxide (NO) can substitute for nitrous oxide (N_2O) in an annealing step within a diffusion furnace at about 900-1000°C.

Oya et al. does not teach a method of forming a gate oxide layer on a semiconductor substrate comprising forming an oxide layer on the substrate by oxidizing the substrate in a

chemical vapor deposition furnace, introducing nitric oxide (NO) gas into the chemical vapor deposition furnace, and nitriding the oxide layer in the presence of the nitric oxide gas.

Neither does Oya et al. teach a method of nitriding a gate oxide layer on a semiconductor substrate comprising nitriding the gate oxide layer in the presence of nitric oxide (NO) gas, wherein the nitriding step is conducted at a temperature of about 800°C or less and at a pressure of about 1 atm or less in a chemical vapor deposition furnace.

Accordingly, Oya et al. fails to anticipate the Claims.

Reconsideration and withdrawal are respectfully requested.

Rejections under 35 U.S.C. § 103

Claims 11, 12, and 23 are rejected under 35 U.S.C. § 103(a) as purportedly unpatentable based on the combination of Oya et al., and Applicants' specification.

Claim 15 is rejected under 35 U.S.C. § 103(a) as purportedly unpatentable based on the combination of Oya et al., and Wu, U.S. Patent No. 6,323,094.

Claim 16 is rejected under 35 U.S.C. § 103(a) as purportedly unpatentable based on Oya et al. alone.

Claim 17 is rejected under 35 U.S.C. § 103(a) as purportedly unpatentable based on the combination of Oya et al. and Van Zant, "Microchip Fabrication, A Practical Guide to Semiconductor Processing" (2000) 4th Ed., McGraw Hill, pgs. 156, 160, 188, 189, 503, 513, and 514.

As noted above, Oya et al. merely discloses nitric oxide (NO) in the context of a heat annealing step that occurs in a diffusion furnace in the first embodiment in Oya et al. and does not teach or suggest a method of forming a gate oxide layer on a semiconductor substrate comprising forming an oxide layer on the substrate by oxidizing the substrate in a chemical vapor

deposition furnace, introducing nitric oxide (NO) gas into the chemical vapor deposition furnace, and nitriding the oxide layer in the presence of the nitric oxide gas. Neither does Oya et al. teach or suggest a method of nitriding a gate oxide layer on a semiconductor substrate comprising nitriding the gate oxide layer in the presence of nitric oxide (NO) gas wherein the nitriding step is conducted at a temperature of about 800°C or less and at a pressure of about 1 atm or less in a chemical vapor deposition furnace.

The secondary references all fail to cure this deficiency in Oya et al.

Reconsideration and withdrawal are respectfully requested.

CONCLUSION

All rejections having been addressed by the present amendments and response, Applicants submit that the present case is in condition for allowance and respectfully request early notice to that effect. If any issues remain to be addressed in this matter which might be resolved by discussion, the Examiner is respectfully requested to call Applicants' undersigned counsel at the number indicated below.

Respectfully submitted,

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MARKED-UP COPY OF PARAGRAPHS, AS AMENDED

Replacement paragraph for second full paragraph at page 3, lines 8-21:

Various nitrogen containing gases have been employed for thermal nitridation and oxy-nitride deposition, [includeing] including N_2, NH_3, NO and N_2O. See, for example, United States Patent Nos. 5,403,786; 5,521,127; [5,629,991] 5,629,221; and 5,880,040. See also Gusev, et al., "Growth and Characterization of Ultrathin Nitrided Silicon Oxide Films", in IBM J. Res. Develop., Vol. 43, No. 3, May 1999, pp. 265-286; Hook, et al., "Nitrided Gate Oxides for 3.3-V Logic Application: Reliability and Device Design Considerations", in IBM J. Res. Develop., Vol. 43, No. 3, May 1999, pp. 393-406; and Buchanan, "Scaling the Gate Dielectric: Materials, Integration and Reliability", in IBM J. Res. Develop., Vol. 43, No. 3, May 1999, pp. 245-264. Evans, et al. disclose a high pressure (15 to 25 atm.) process for oxynitride gate formation using nitric oxide gas. See Evans, et al., "High Performance CMOS Devices with 20 Å Engineered Oxynitride Gate Dielectrics", Paper Presented at Semicon Korea Technical Symposium, (February 2000).